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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/472,869	12/28/1999	Tae-Yong Sohn	Q57124	9316

7590 05/12/2003

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EXAMINER

NATNAEL, PAULOS M

ART UNIT

PAPER NUMBER

2614

DATE MAILED: 05/12/2003

13

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	09/472,869	SOHN, TAE-YONG	
	Examiner Paulos M. Natnael	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 30 October 2002.

2a) This action is FINAL.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) 1-4 and 11 is/are allowed.

6) Claim(s) 5 is/are rejected.

7) Claim(s) 6-9 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing-Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.

4) Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

**DETAILED ACTION**

1. The Final Rejection has been withdrawn. The previously indicated allowability of Claim 5 has been also withdrawn.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seino et al. U.S. Pat. No. 6,384,867.

Considering claim 5,

b) the claimed analog to digital converter for converting a received analog video signal into a second input digital signal is met by A/D converter 22, Fig.1;

c) the claimed a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal into a predetermined display format output signal is met format converter 21, fig.1;

- d) the claimed controller for detecting a frame rate of the input digital signal received by said format converter and outputting a timing control signal corresponding to the frame rate detected is met by the automatic discrimination circuit 1, fig. 1;
- e) the clock frequency providing means for providing a clock frequency according to the timing control signal output by said controller, said clock frequency provided to the format converter for converting the input digital signal received by said format converter into said predetermined display output signal, said clock frequency also provided to said video decoder when said second input digital signal is not present at said format converter is met by PLL-control-signal Generation circuit 2, fig.1;

Except for;

- a) the claimed video decoder for decoding a video component of a received digital signal into a first input digital signal;

Regarding a), Seino et al. discloses a decoder in the automatic discrimination circuit 1. Seino et al. Does not specifically disclose a video decoder in the video signal reception circuit. However, it would be obvious to the skilled in the art , the video signal received in the A/D conversion circuit must be decoded before being further processed further in the system. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Seino et al. by adding a video decoder after the A/D conversion circuit in order to properly process and display the received video signal.

***Allowable Subject Matter***

1. Claims 1-4 are allowed.
2. Claims 6-9 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
3. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a first PLL circuit and a second PLL circuit, a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal into a predetermined display format output signal, and a controller for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of the input digital signal, as in claims 1;

Wherein the step of selecting the clock frequency comprises, outputting a control signal from a controller, said control signal depending upon the frame rate which is detected; receiving said control signal into a selector, said selector connected to outputs of a plurality of phase locked loops, wherein each phase locked loop has a predetermined clock frequency, and selecting one predetermined clock frequency of one of said plurality of phase locked loops based upon the control signal received by the selector, as in claim 11.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703)305-0019. The examiner can normally be reached on 6:30am -3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703)305-4795. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Paulos M. Natnael  
May 5, 2003

*Pmn*